# EE105 – Fall 2015
# Microelectronic Devices and Circuits
## Multi-Stage Amplifiers

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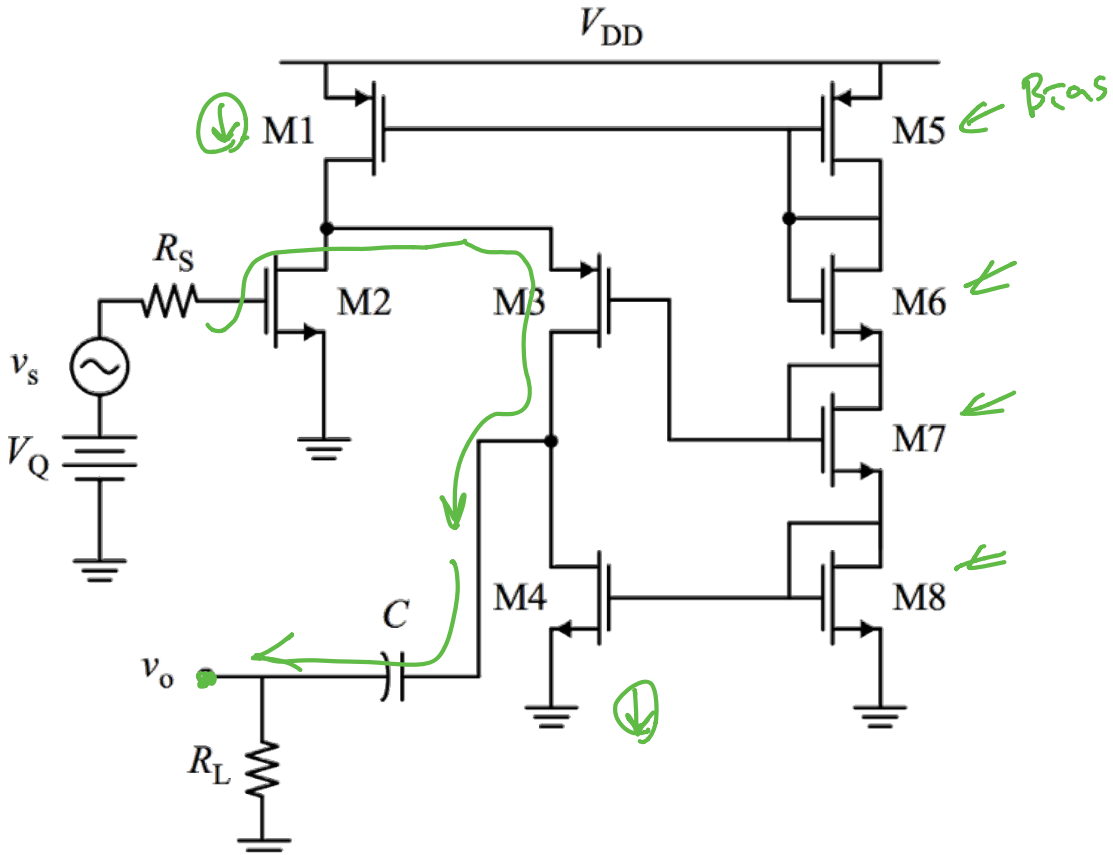
# Example of Multi-Stage Amplifier

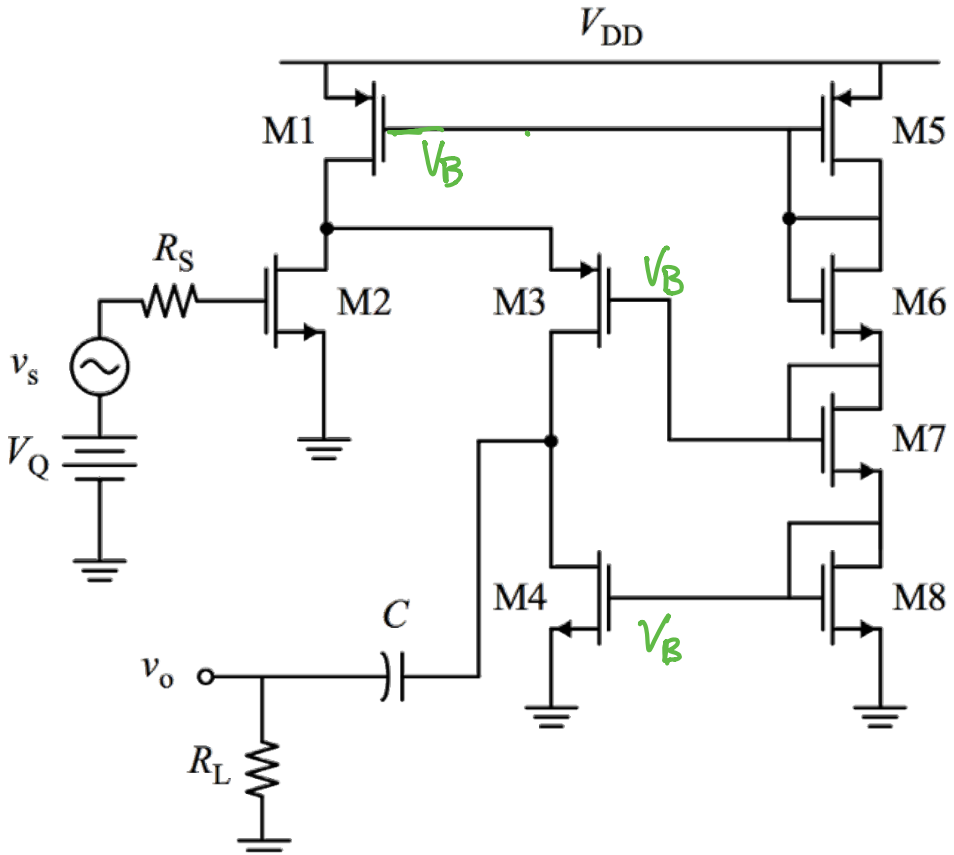


# Cutting Through the Complexity

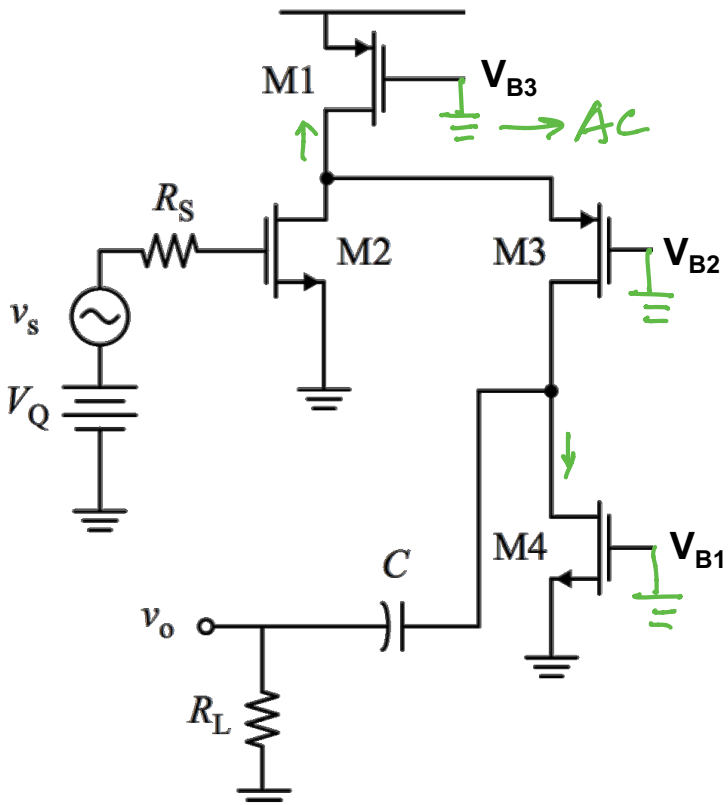
1. Identify the "signal path" between the input and output
2. Eliminate "background" transistors to reduce clutter
3. For "background transistors, understand their role (e.g. DC biasing)
4. For frequency response, identify "hi-Z" nodes.



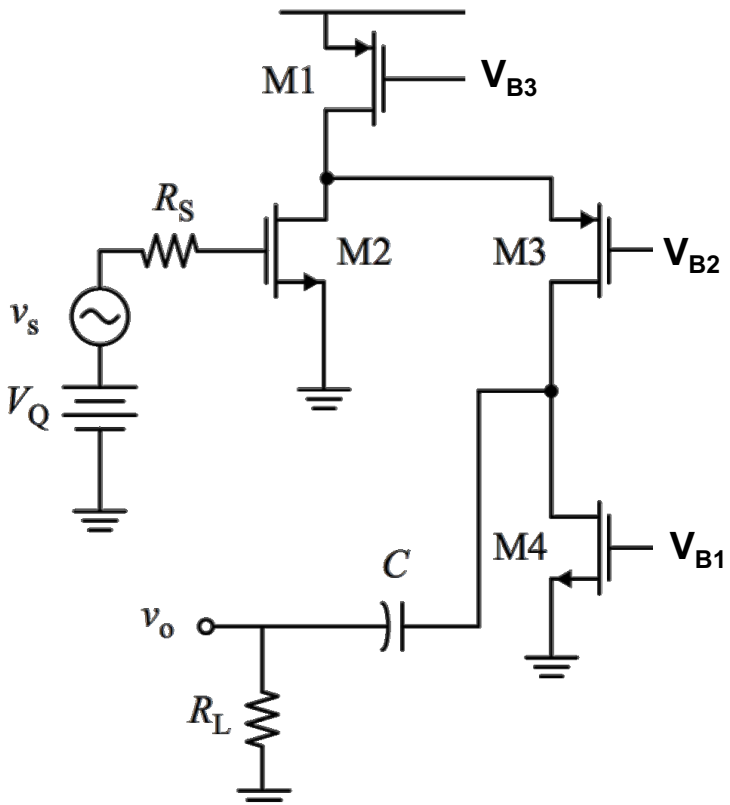
# Eliminate Clutter



# Identify Signal Path & Amplifier Stages

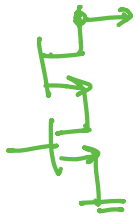


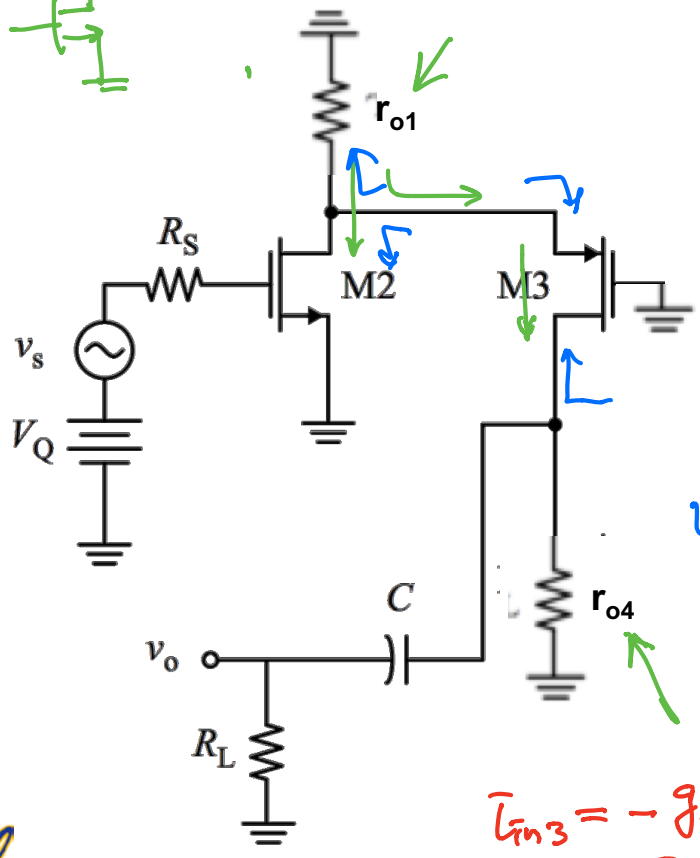
# DC Biasing



# Small-Signal Models

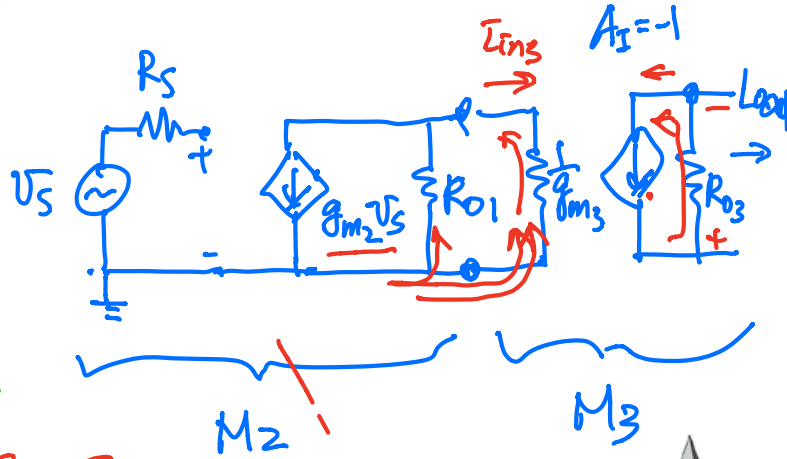
CS + CG = Folded Cascode






$R_{o1} = r_{o1} \parallel r_{o2}$

$R_{o3} = g_{m3} r_{o3} R_{o1}$


$i_{in3} = -g_{m2} v_s$

$i_{out} = -i_{in3} = +g_{m2} v_s$

Without Load: $v_{out} = -i_{out} R_{o3} = g_{m2} v_s \cdot g_{m3} r_{o3} \cdot (r_{o1} \parallel r_{o2})$

$\Rightarrow A_v = g_{m2} g_{m3} r_{O3} \cdot (r_{O1} /\!/ r_{O2})$

# Two-Port Model



# External Loads

- Many applications must drive external loads that are very low impedance compared to on-chip levels
- These stages must drive high voltages/currents so linearity is a concert. We must consider "large signal" behavior
- Example: Speaker at 8 ohms versus Megaohms on-chip …
- Follower is natural choice, but it can only "source" current (think in terms of large signals)


# Design Issue: DC Coupling

- **Constraint: large inductors and capacitors are not available**
- **Output of one stage is directly connected to the input of the next stage → must consider DC levels … why?**